

74ALVCH16374

Low-Voltage 16-Bit D-Type Flip-Flop with Bus Hold 1.8/2.5/3.3 V (3-State, Non-Inverting)

The 74ALVCH16374 is an advanced performance, non-inverting 16-bit D-type flip-flop. It is designed for very high-speed, very low-power operation in 1.8 V, 2.5 V or 3.3 V systems. The VCXH16374 is byte controlled, with each byte functioning identically, but independently. Each byte has separate Output Enable and Clock Pulse inputs. These control pins can be tied together for full 16-bit operation.

The 74ALVCH16374 consists of 16 edge-triggered flip-flops with individual D-type inputs and 3.6 V-tolerant 3-state outputs. The clocks (CPn) and Output Enables ($\overline{OE}n$) are common to all flip-flops within the respective byte. The flip-flops will store the state of individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the \overline{OE} LOW, the contents of the flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. The \overline{OE} input level does not affect the operation of the flip-flops. The data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating inputs at a valid logic state.

- Designed for Low Voltage Operation: $V_{CC} = 1.65 - 3.6$ V
- 3.6 V Tolerant Inputs and Outputs
- High Speed Operation: 3.6 ns max for 3.0 to 3.6 V
4.5 ns max for 2.3 to 2.7 V
7.8 ns max for 1.65 to 1.95 V
- Static Drive: ± 24 mA Drive at 3.0 V
 ± 12 mA Drive at 2.3 V
 ± 4 mA Drive at 1.65 V
- Supports Live Insertion and Withdrawal
- Includes Active Bushold to Hold Unused or Floating Inputs at a Valid Logic State
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0$ V†
- Near Zero Static Supply Current in All Three Logic States (40 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds ± 250 mA @ 125°C
- ESD Performance: Human Body Model >2000V; Machine Model >200V
- Second Source to Industry Standard 74ALVCH16374

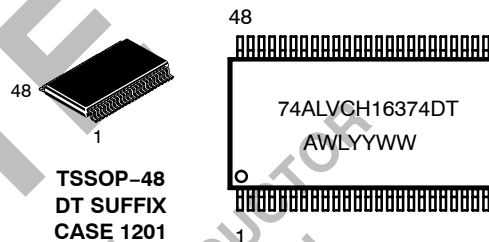
†To ensure the outputs activate in the 3-state condition, the output enable pins should be connected to V_{CC} through a pull-up resistor. The value of the resistor is determined by the current sinking capability of the output connected to the OE pin.



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MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN NAMES

| Pins | Function |
|------------------|----------------------|
| $\overline{OE}n$ | Output Enable Inputs |
| CPn | Clock Pulse Inputs |
| D0-D15 | Inputs |
| O0-O15 | Outputs |

ORDERING INFORMATION

| Device | Package | Shipping |
|-----------------|---------|-------------|
| 74ALVCH16374DTR | TSSOP | 2500 / Reel |

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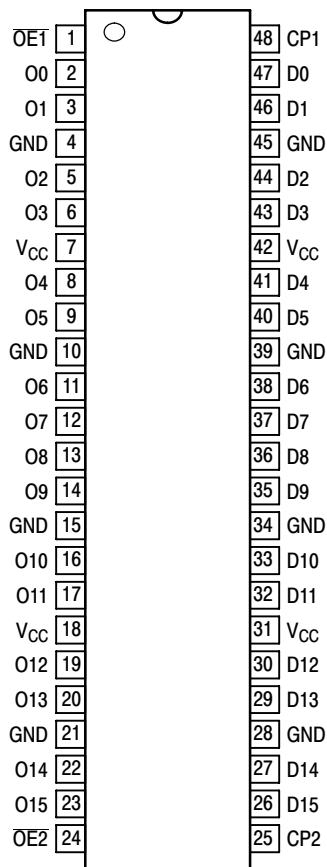


Figure 1. 48-Lead Pinout (Top View)

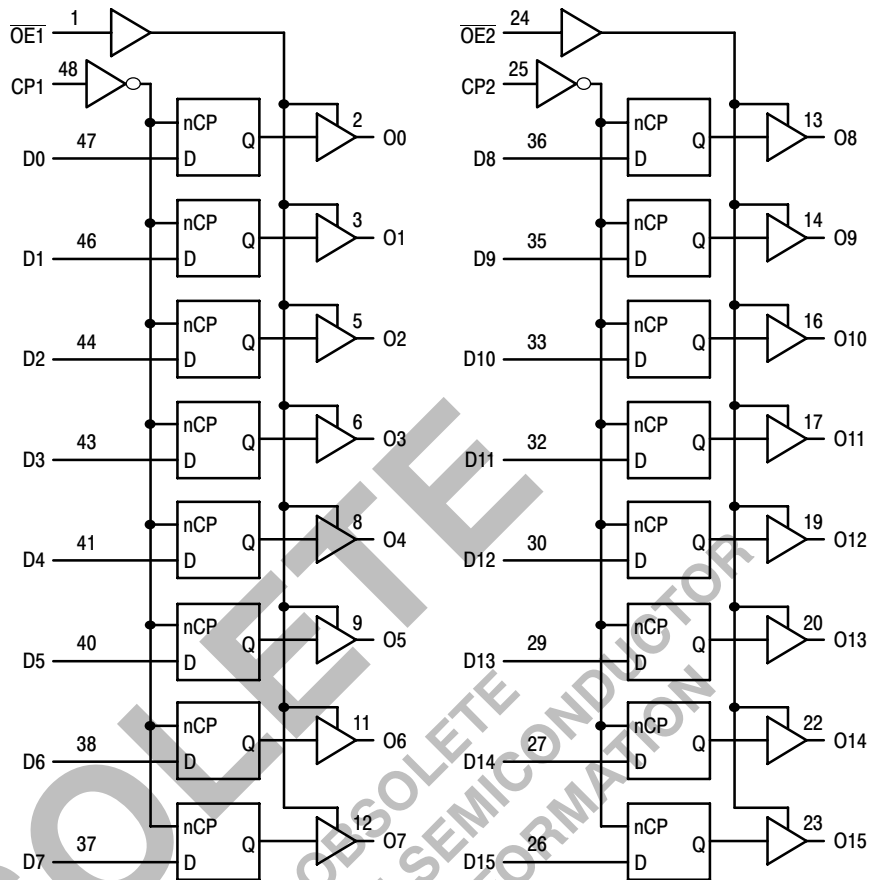


Figure 2. Logic Diagram

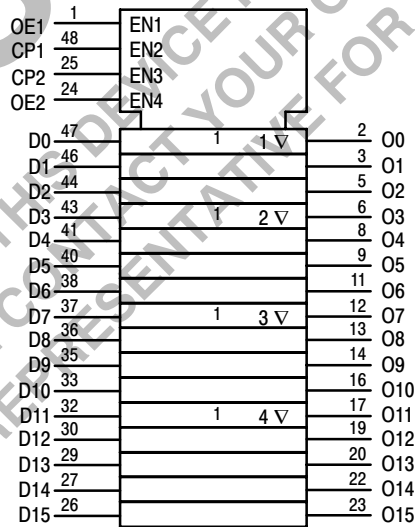


Figure 3. IEC Logic Diagram

| Inputs | | | Outputs | Inputs | | | Outputs |
|--------|-----|------|---------|--------|-----|-------|---------|
| CP1 | OE1 | D0:7 | O0:7 | CP2 | OE2 | D8:15 | O8:15 |
| ↑ | L | H | H | ↑ | L | H | H |
| ↑ | L | L | L | ↑ | L | L | L |
| X | L | X | O0 | X | L | X | O0 |
| X | H | X | Z | X | H | X | Z |

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; ↑ = Low-to-High Transition; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs. O0 = No Change.

MAXIMUM RATINGS (Note 1)

| Symbol | Parameter | Value | Unit |
|-----------------------|---|------------------------|------|
| V _{CC} | DC Supply Voltage | - 0.5 to + 4.6 | V |
| V _I | DC Input Voltage | - 0.5 to + 4.6 | V |
| V _O | DC Output Voltage | - 0.5 to + 4.6 | V |
| I _{IK} | DC Input Diode Current V _I < GND | - 50 | mA |
| I _{OK} | DC Output Diode Current V _O < GND | - 50 | mA |
| I _O | DC Output Sink Current | ± 50 | mA |
| I _{CC} | DC Supply Current per Supply Pin | ± 100 | mA |
| I _{GND} | DC Ground Current per Ground Pin | ± 100 | mA |
| T _{STG} | Storage Temperature Range | - 65 to + 150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| T _J | Junction Temperature Under Bias | + 150 | °C |
| θ _{JA} | Thermal Resistance (Note 2) | 90 | °C/W |
| MSL | Moisture Sensitivity | Level 1 | |
| F _R | Flammability Rating Oxygen Index: 30 to 35 | UL 94 V-O @ 0.125 in | |
| V _{ESD} | ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5) | > 2000 > 200 N/A | V |
| I _{LATCH-UP} | Latch-Up Performance Above V _{CC} and Below GND at 125°C (Note 6) | ± 250 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-----------------|--|------------|------------|------|
| V _{CC} | Supply Voltage Operating Data Retention Only | 2.3 1.5 | 3.6 3.6 | V |
| V _I | Input Voltage (Note 7) | -0.5 | 3.6 | V |
| V _O | Output Voltage (Active State) (3-State) | 0 0 | 3.6 3.6 | V |
| T _A | Operating Free-Air Temperature | - 40 | + 85 | °C |
| Δt/ΔV | Input Transition Rise or Fall Rate V _{CC} = 2.5 V ± 0.2 V V _{CC} = 3.0 V ± 0.3 V | 0 0 | 20 10 | ns/V |

7. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

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DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Condition | T _A = -40°C to +85°C | | Unit |
|----------------------|---------------------------------------|---|---------------------------------|------------------------|------|
| | | | Min | Max | |
| V _{IH} | HIGH Level Input Voltage (Note 8) | 1.65 V ≤ V _{CC} < 2.3 V | 0.65 × V _{CC} | | V |
| | | 2.3 V ≤ V _{CC} ≤ 2.7 V | 1.7 | | |
| | | 2.7 V < V _{CC} ≤ 3.6 V | 2.0 | | |
| V _{IL} | LOW Level Input Voltage (Note 8) | 1.65 V ≤ V _{CC} < 2.3 V | | 0.35 × V _{CC} | V |
| | | 2.3 V ≤ V _{CC} ≤ 2.7 V | | 0.7 | |
| | | 2.7 V < V _{CC} ≤ 3.6 V | | 0.8 | |
| V _{OH} | HIGH Level Output Voltage | 1.65 V ≤ V _{CC} ≤ 3.6 V; I _{OH} = -100 μA | V _{CC} - 0.2 | | V |
| | | V _{CC} = 1.65 V; I _{OH} = -4 mA | 1.2 | | |
| | | V _{CC} = 2.3 V; I _{OH} = -6 mA | 2.0 | | |
| | | V _{CC} = 2.3 V; I _{OH} = -12 mA | 1.7 | | |
| | | V _{CC} = 2.7 V; I _{OH} = -12 mA | 2.2 | | |
| | | V _{CC} = 3.0 V; I _{OH} = -12 mA | 2.4 | | |
| | | V _{CC} = 3.0 V; I _{OH} = -24 mA | 2.0 | | |
| V _{OL} | LOW Level Output Voltage | 1.65 V ≤ V _{CC} ≤ 3.6 V; I _{OL} = 100 μA | | 0.2 | V |
| | | V _{CC} = 1.65 V; I _{OL} = 4 mA | | 0.45 | |
| | | V _{CC} = 2.3 V; I _{OL} = 6 mA | | 0.4 | |
| | | V _{CC} = 2.3 V; I _{OL} = 12 mA | | 0.7 | |
| | | V _{CC} = 2.7 V; I _{OL} = 12 mA | | 0.4 | |
| | | V _{CC} = 3.0 V; I _{OL} = 24 mA | | 0.55 | |
| I _I | Input Leakage Current | 1.65 V ≤ V _{CC} ≤ 3.6 V; 0 V ≤ V _I ≤ 3.6 V | | ± 5.0 | μA |
| I _{I(HOLD)} | Minimum Bus-hold Input Current | V _{CC} = 3.6 V; V _{IN} = 0 to 3.6 V | | ± 500 | μA |
| | | V _{CC} = 3.0 V, V _{IN} = 0.8 V | 75 | | |
| | | V _{CC} = 3.0 V, V _{IN} = 2.0 V | -75 | | |
| | | V _{CC} = 2.3 V, V _{IN} = 0.7 V | 45 | | |
| | | V _{CC} = 2.3 V, V _{IN} = 1.7 V | -45 | | |
| | | V _{CC} = 1.65 V, V _{IN} = 0.58 V | 25 | | |
| | | V _{CC} = 1.65 V, V _{IN} = 1.07 V | -25 | | |
| I _{OZ} | 3-State Output Current | 1.65 V ≤ V _{CC} ≤ 3.6 V; 0 V ≤ V _O ≤ 3.6 V; V _I = V _{IH} or V _{IL} | | ± 10 | μA |
| I _{OFF} | Power-Off Leakage Current | V _{CC} = 0 V; V _I or V _O = 3.6 V | | 10 | μA |
| I _{CC} | Quiescent Supply Current (Note 9) | 1.65 V ≤ V _{CC} ≤ 3.6 V; V _I = GND or V _{CC} | | 40 | μA |
| | | 1.65 V ≤ V _{CC} ≤ 3.6 V; 3.6 V ≤ V _I , V _O ≤ 3.6 V | | ± 40 | |
| ΔI _{CC} | Increase in I _{CC} per Input | 2.7 V < V _{CC} ≤ 3.6 V; V _{IH} = V _{CC} - 0.6 V | | 750 | μA |

8. These values of V_I are used to test DC electrical characteristics only.

9. Outputs disabled or 3-state only.

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AC CHARACTERISTICS (Note 10; $t_R = t_F = 2.0$ ns; $C_L = 30$ pF; $R_L = 500 \Omega$)

| Symbol | Parameter | Wave-form | Limits | | | | | | Unit |
|--------------------------|--|-----------|---|------------|-----------------------------|------------|-------------------------------|--------------|------|
| | | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | | | | | |
| | | | $V_{CC} = 3.0$ V to 3.6 V | | $V_{CC} = 2.3$ V to 2.7 V | | $V_{CC} = 1.65$ V to 1.95 V | | |
| | | | Min | Max | Min | Max | Min | Max | |
| f_{max} | Clock Pulse Frequency | 1 | 250 | | 200 | | 100 | | MHz |
| t_{PLH} t_{PHL} | Propagation Delay CP to On | 1 | 1.0 1.0 | 3.6 3.6 | 1.0 1.0 | 4.5 4.5 | 1.0 1.0 | 7.8 7.8 | ns |
| t_{PZH} t_{PZL} | Output Enable Time to High and Low Level | 2 | 1.0 1.0 | 4.7 4.7 | 1.0 1.0 | 6.0 6.0 | 1.0 1.0 | 9.2 9.2 | ns |
| t_{PHZ} t_{PLZ} | Output Disable Time From High and Low Level | 2 | 1.0 1.0 | 4.1 4.1 | 1.0 1.0 | 5.1 5.1 | 1.5 1.5 | 6.8 6.8 | ns |
| t_s | Setup Time, High or Low Dn to CP | 3 | 1.5 | | 0.5 | | 2.5 | | ns |
| t_h | Hold Time, High or Low Dn to CP | 3 | 1.0 | | 0.5 | | 1.0 | | ns |
| t_w | CP Pulse Width, High | 3 | 1.5 | | 0.5 | | 4.0 | | ns |
| t_{OSHL} t_{OSLH} | Output-to-Output Skew (Note 11) | | | 0.5 0.5 | | 0.5 0.5 | | 0.75 0.75 | ns |

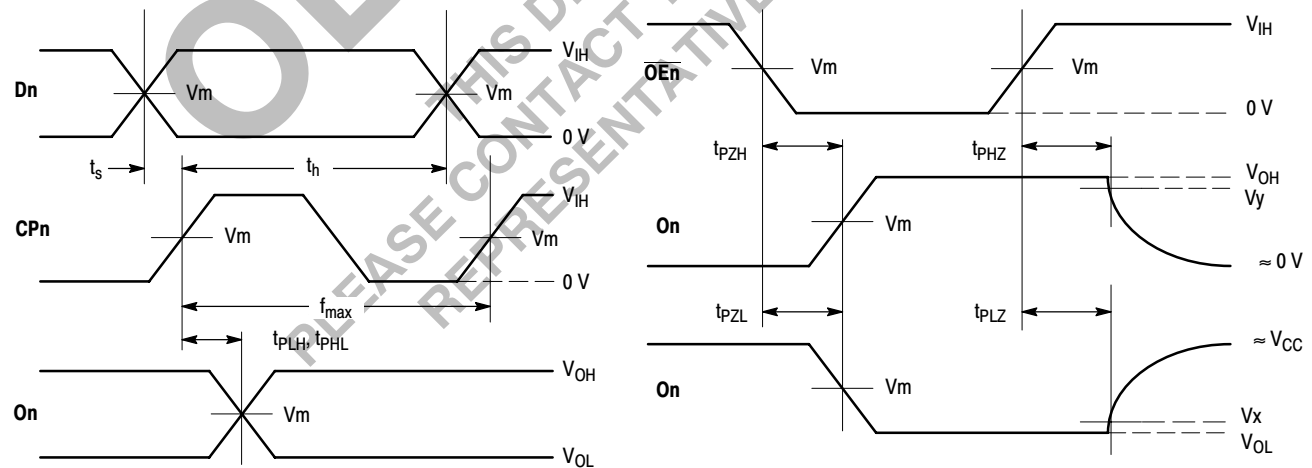
10. For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.

11. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typical | Unit |
|-----------|-------------------------------|-----------------|---------|------|
| C_{IN} | Input Capacitance | Note 12 | 6 | pF |
| C_{OUT} | Output Capacitance | Note 12 | 7 | pF |
| C_{PD} | Power Dissipation Capacitance | Note 12, 10 MHz | 20 | pF |

12. $V_{CC} = 1.8, 2.5$ or 3.3 V; $V_I = 0$ V or V_{CC} .

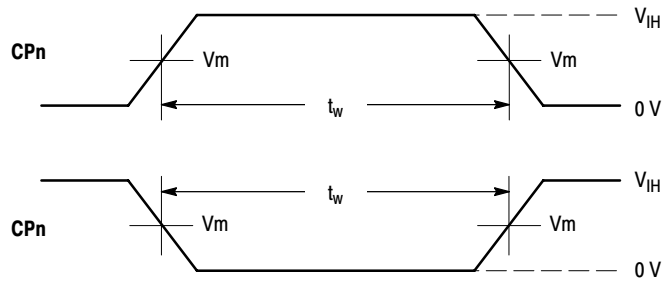


WAVEFORM 1 - PROPAGATION DELAYS, SETUP AND HOLD TIMES
 $t_R = t_F = 2.0$ ns, 10% to 90%; $f = 1$ MHz; $t_w = 500$ ns

WAVEFORM 2 - OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.0$ ns, 10% to 90%; $f = 1$ MHz; $t_w = 500$ ns

Figure 4. AC Waveforms

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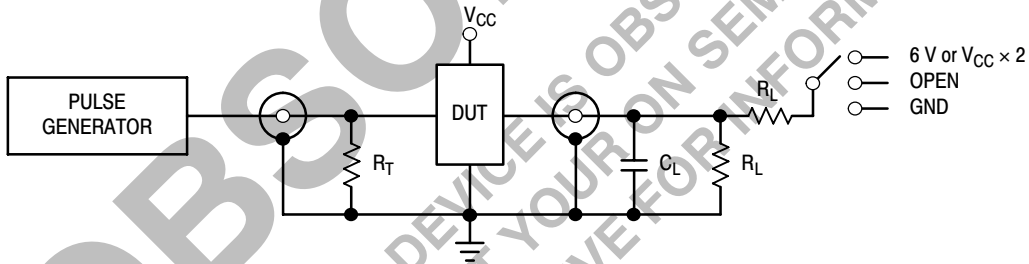


WAVEFORM 3 - PULSE WIDTH

$t_R = t_F = 2.0 \text{ ns}$ (or fast as required) from 10% to 90%

Figure 5. AC Waveforms

| Symbol | V_{CC} | | |
|----------|-----------------------------------|-----------------------------------|------------------------------------|
| | $3.3 \text{ V} \pm 0.3 \text{ V}$ | $2.5 \text{ V} \pm 0.2 \text{ V}$ | $1.8 \text{ V} \pm 0.15 \text{ V}$ |
| V_{IH} | 2.7 V | V_{CC} | V_{CC} |
| V_m | 1.5 V | $V_{CC}/2$ | $V_{CC}/2$ |
| V_x | $V_{OL} + 0.3 \text{ V}$ | $V_{OL} + 0.15 \text{ V}$ | $V_{OL} + 0.15 \text{ V}$ |
| V_y | $V_{OH} - 0.3 \text{ V}$ | $V_{OH} - 0.15 \text{ V}$ | $V_{OH} - 0.15 \text{ V}$ |



| TEST | SWITCH |
|--------------------|--|
| t_{PLH}, t_{PHL} | Open |
| t_{PZL}, t_{PLZ} | 6 V at $V_{CC} = 3.3 \pm 0.3 \text{ V}$; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2 \text{ V}; 1.8 \text{ V} \pm 0.15 \text{ V}$ |
| t_{PZH}, t_{PHZ} | GND |

$C_L = 50 \text{ pF}$ for $V_{CC} = 3.0 \pm 0.3 \text{ V}$

$R_L = 500 \Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 6. Test Circuit

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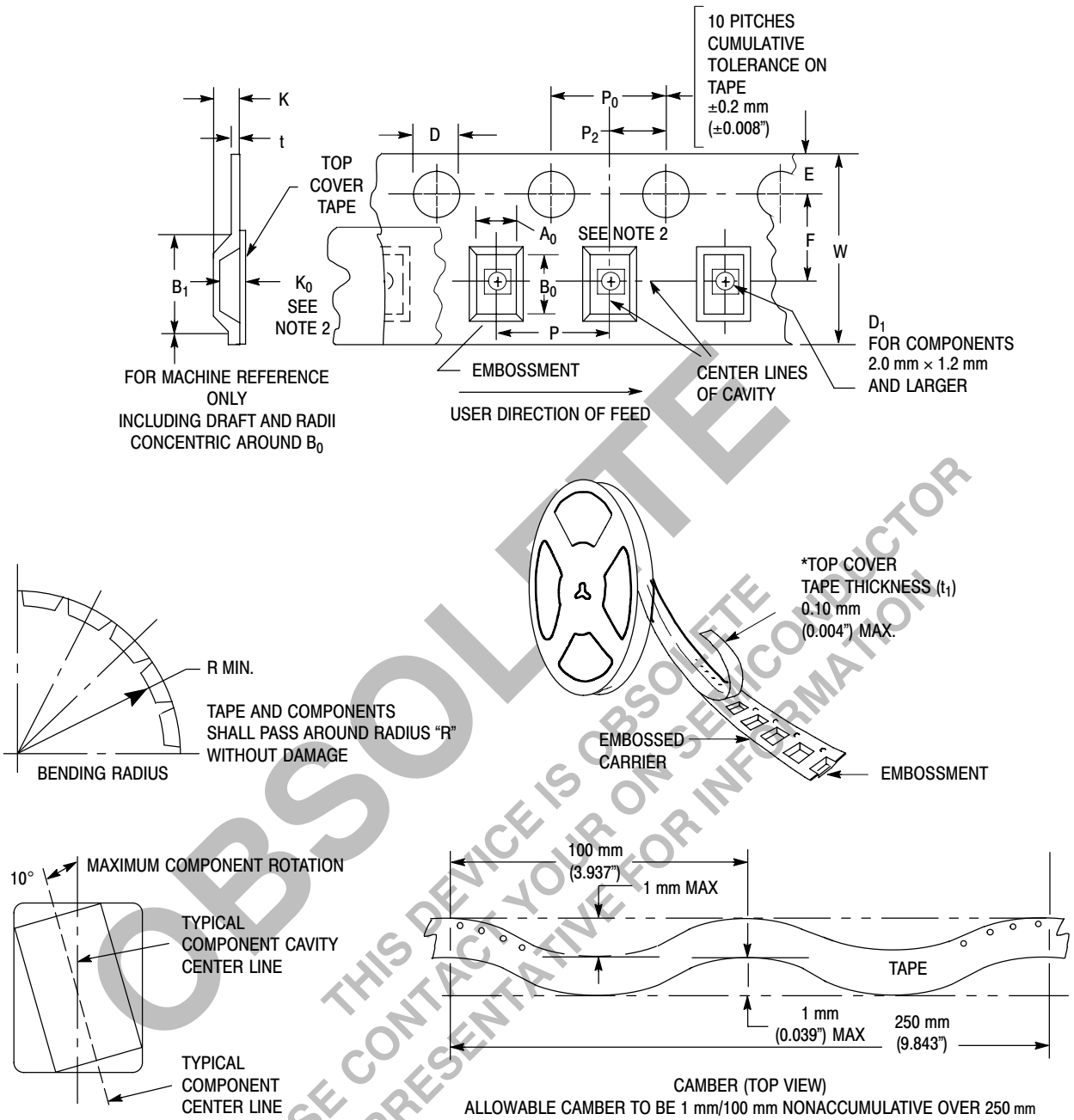


Figure 7. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 1 and 2)

| Tape Size | B_1 Max | D | D_1 | E | F | K | P | P_0 | P_2 | R | T | W |
|-----------|-----------------|---------------------------------------|--------------------|--|---|----------------------|---|---|---|---------------|-----------------|------------------|
| 24mm | 20.1mm (0.791") | 1.5 + 0.1mm -0.0 (0.059 +0.004" -0.0) | 1.5mm Min (0.060") | 1.75 ± 0.1 mm (0.069 ± 0.004 ") | 11.5 ± 0.10 mm (0.453 ± 0.004 ") | 11.9 mm Max (0.468") | 16.0 ± 0.1 mm (0.63 ± 0.004 ") | 4.0 ± 0.1 mm (0.157 ± 0.004 ") | 2.0 ± 0.1 mm (0.079 ± 0.004 ") | 30 mm (1.18") | 0.6 mm (0.024") | 24.3 mm (0.957") |

13. Metric Dimensions Govern—English are in parentheses for reference only.

14. A_0 , B_0 , and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity.

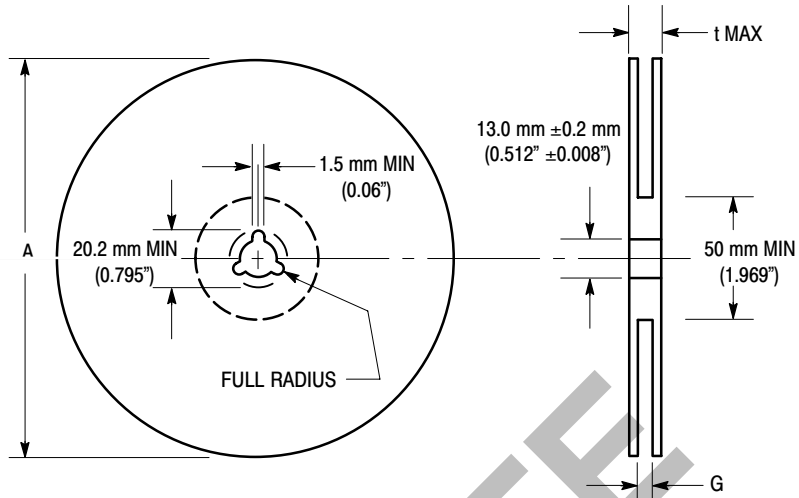


Figure 8. Reel Dimensions

REEL DIMENSIONS

| Tape Size | A Max | G | t Max |
|-----------|---------------------|--|---------------------|
| 24 mm | 360 mm (14.173") | 24.4 mm + 2.0 mm, -0.0 (0.961" + 0.078", -0.00) | 30.4 mm (1.197") |

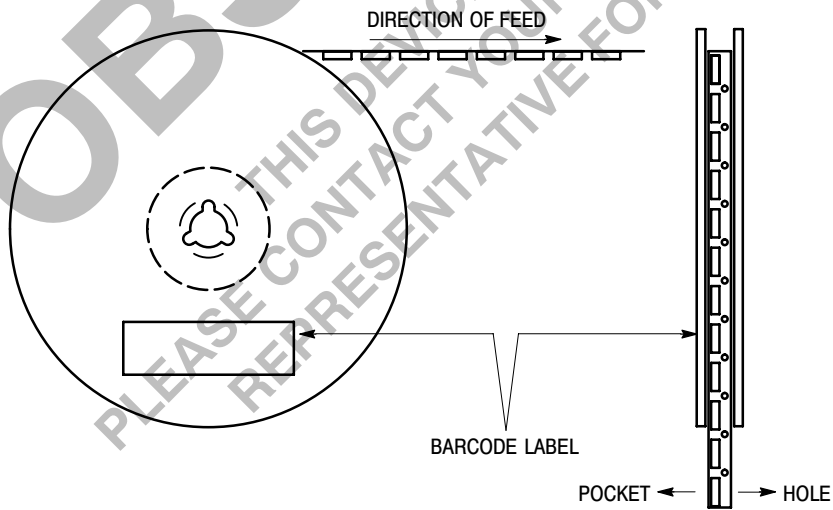


Figure 9. Reel Winding Direction

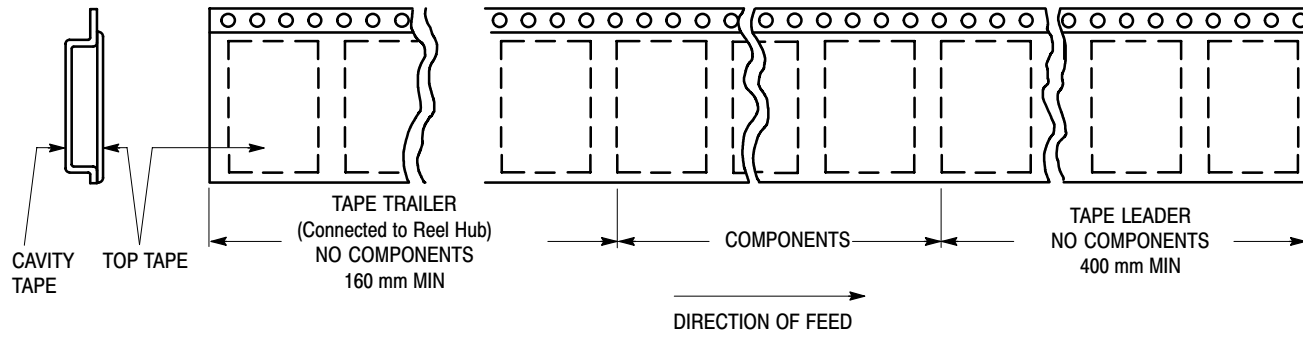


Figure 10. Tape Ends for Finished Goods

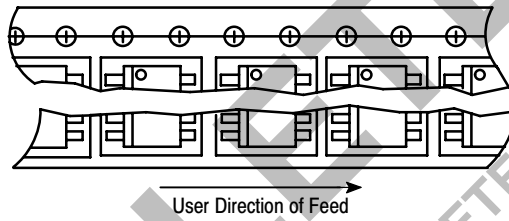


Figure 11. Reel Configuration

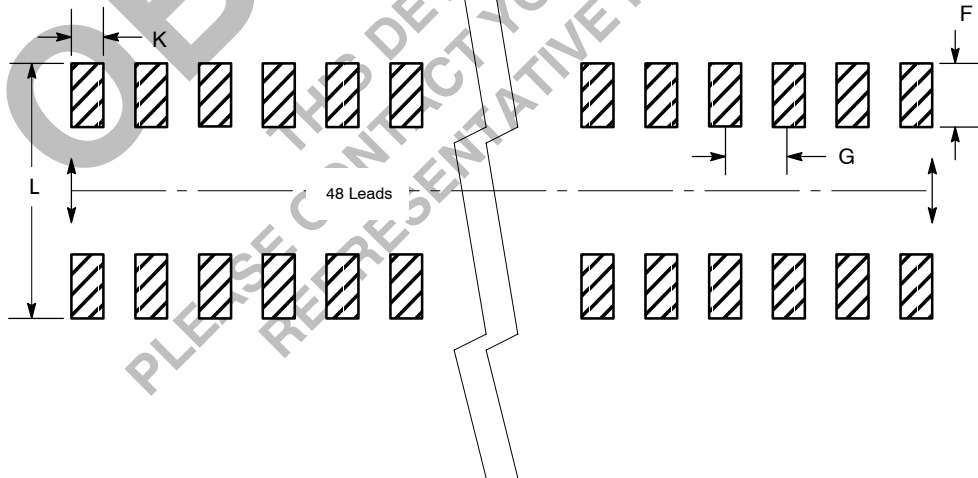
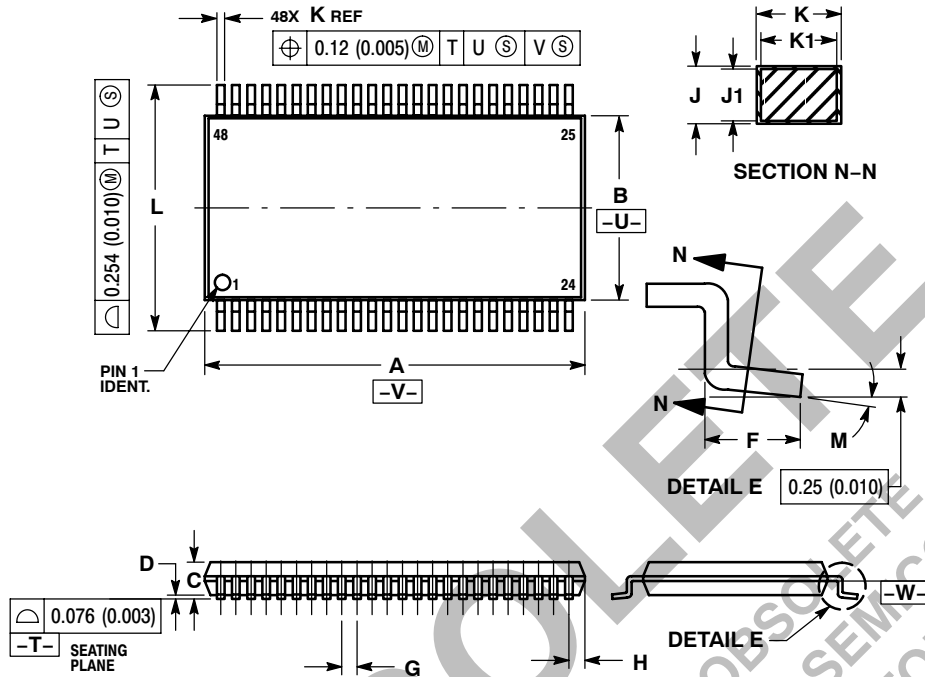


Figure 12. Package Footprint

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PACKAGE DIMENSIONS

TSSOP
DT SUFFIX
CASE 1201-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 12.40 | 12.60 | 0.488 | 0.496 |
| B | 6.00 | 6.20 | 0.236 | 0.244 |
| C | --- | 1.10 | --- | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.50 BSC | | 0.0197 BSC | |
| H | 0.37 | --- | 0.015 | --- |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.17 | 0.27 | 0.007 | 0.011 |
| K1 | 0.17 | 0.23 | 0.007 | 0.009 |
| L | 7.95 | 8.25 | 0.313 | 0.325 |
| M | 0° | 8° | 0° | 8° |

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